CLAIMS

1. A DC amplifier formed on a substrate of a semiconductor integrated circuit, comprising

a differential amplification circuit including a MIS field-effect transistor in which a projecting portion is formed by a silicon substrate having a first crystal surface as a primary surface and a second crystal surface as a side surface, terminated hydrogen on the silicon surface is removed in plasma atmosphere of an inert gas, then a gate insulating film is formed on at least a part of a top surface and the side surface of the projecting portion at a temperature at or lower than about 550°C in the plasma atmosphere, a gate is formed on the gate insulating film, and a drain and a source are formed on both sides enclosing the gate insulating film of the projecting portion.

2. The DC amplifier according to claim 1, wherein

a channel is formed on the first crystal surface of a top surface and the second crystal surface of the side surface of the projecting portion, and the channel width of the MIS field-effect transistor is a total of a channel width of the top surface and a channel width of the side surface.

3. The DC amplifier according to claim 1 or 2, wherein the projecting portion has the top surface comprising a silicon surface (100), the side surface comprising a silicon surface (110), and the source and drain are formed on the projecting portion enclosing the gate and in left and right areas of the projecting portion of the silicon substrate.

4. The DC amplifier according to claim 1 or 2, further comprising first and second MIS field-effect transistors for performing differential amplification on an input signal, and a third MIS field-effect transistor which is connected to a source or a drain of the first and second MIS field-effect transistors and configures a constant current circuit.

5. The DC amplifier according to claim 4, further comprising fourth and fifth MIS field-effect transistors which are connected between a source or a drain of the first and second MIS field-effect transistors and configure a constant current circuit as a load of the first and second MIS field-effect transistors.

6. A semiconductor integrated circuit, comprising on a same circuit substrate:

a circuit including a p-channel MIS field-effect transistor and an n-channel MIS field-effect transistor in which a projecting portion is formed by a silicon substrate having a first crystal surface as a primary surface and a second crystal surface as a side surface, terminated hydrogen on the silicon surface is removed in plasma atmosphere of an inert gas, then a gate insulating film is formed on at least a part of the top surface and the side surface of the projecting portion at a temperature at or lower than about 550°C in the plasma atmosphere, a gate is formed on the gate insulating film, and a drain and a source are formed on both sides enclosing the gate insulating film of the projecting portion; and

a DC amplifier having a differential amplification circuit including the p-channel MIS field-effect transistor or the n-channel MIS field-effect transistor.

7. The semiconductor integrated circuit according to claim 6, wherein

gate widths of a top surface and a side surface of the p-channel MIS field-effect transistor and the

n-channel MIS field-effect transistor are set such that the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor.

8. The semiconductor integrated circuit according to claim 6 or 7, wherein

the limiter circuit comprises a CMOS circuit having the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor.